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U.S. UTILITY Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10090239	03/01/2002	326	41	2819	Anh Tran

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**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐

Foreign priority claimed	☐ yes ☒ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☒ no	X-1061 US
Verified and Acknowledged Examiners's intials	AT	

TITLE : Low jitter clock for a physical media access sublayer on a field programmable gate array

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
10/28/03	Assistant Examiner	Total Claims: 58	Print Claim for O.G: 1
ISSUE FEE		**DRAWING**	
Amount Due: $1330	Date Paid:	Sheets Drwg.: 4	Figs.Drwg.: 4
	ANH TRAN		Print Fig.: 2
☐ TERMINAL DISCLAMER	Primary Examiner 10/24/03 PREPARED FOR ISSUE	Application Examiner	

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